Dr. Vrajesh D. Maheta (PhD)
Associate Professor

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Building No: A4, Flat No: 05, Plot No 3A,

Balaji Krupa CHS, Sector-28,

Nerul, Navi Mumbai, Thane.

Maharashtra- 400706

Professional Qualification:

- **Ph.D in Electrical Engineering, 2009**
  Indian Institute of Technology Bombay, Mumbai
- **Master of Microelectronics Engineering in 2003**
  Birla Institute of Technology & Science, Pilani
- **Bachelor of Electronics Engineering, 1997**
  Birla Vishwakarma Mahavidyalaya, Sardar Patel University, Vallabhvidyanagar, Gujarat

Short Biodata:

Dr. Vrajesh is having more than eighteen years of teaching experience at under graduate level and more than three years of teaching experience at post graduate level in various engineering institutes. He has published seven technical papers in referred international journals and fifteen technical papers in referred international conference proceedings. He has conducted, organized and attended several technical workshops in the field of VLSI and SoPC Design. His research area includes Advanced CMOS device reliability, Device characterization, Digital system design using CPLD/FPGA and System on Programmable Chip (SoPC) Design.

Major Subjects:

- Digital VLSI Design, ASIC Design, VLSI Techniques, Semi-conductor Devices, Microcontroller and Embedded Programming, Computer Organization and Architecture, Digital Logic Design, Electronic circuits, Semi-conductor device physics, Network Analysis, Electronic Measurement, Electromagnetic fields, Basic Electronics Engineering, Digital VLSI Lab, IOT Lab, Sensor Network Lab, Microprocessor Lab and UG Projects.

Citation Analysis:

639 citations (h-index 14 and i10-index 14) in google scholar

https://scholar.google.com/citations?user=XflT0IsAAAAJ&hl=en

List of Publication:

Journal Publications:

1. A. E. Islam, S. Mahapatra, S. Deora, V. D. Maheta and M. A. Alam, "Essential Aspects of Negative Bias Temperature Instability", (invited) ECS Trans., vol. 35, no. 4, pp. 145-174, 2011.

2. S. Deora, V. D. Maheta, A. E. Islam, M. A. Alam and S. Mahapatra, " A common framework of NBTI generation and recovery in Plasma nitrided SiON p-MOSFETs", IEEE Electron Device Lett., vol. 30, no. 9, pp. 978-980, Sept. 2009, ISSN: 0741-3106.
3. S. Mahapatra, V. D. Maheta, S. Deora, E. N. Kumar, S. Purawat, C. Olsen, K. Ahmed, A. E. Islam and M. A. Alam, "Material dependence of Negative Bias Temperature Instability (NBTI) stress and Recovery in SiON p-MOSFETs", ECS Trans., vol. 19, no. 2, pp. 243-263, May 2009.
4. S. Deora, V. D. Maheta, G. Bersuker, C. Olsen, K. Z. Ahmed, R. Jammy and S. Mahapatra, "A comparative NBTI study of HfO2, HfSiOx, and SiON p-MOSFETs using UF-OTF IDLIN Technique", IEEE Electron Device Lett., vol. 30, no. 2, pp. 152-154, Feb. 2009, ISSN: 0741-3106.
5. S. Mahapatra, V. D. Maheta, A. E. Islam and M. A. Alam, "Isolation of NBTI Stress Generated Interface Trap and Hole Trapping Components in PNO p-MOSFETs,", IEEE Trans. Electron Devices, vol. 56, no. 2, pp. 236-242, Feb. 2009, ISSN: 0018-9383.
6. V. D. Maheta, E. N. Kumar, S. Purawat, C. Olsen, K. Ahmed and S. Mahapatra, "Development of an Ultra-Fast On-The-Fly IDLIN Technique to Study NBTI in Plasma and Thermal Oxynitride p-MOSFETs," IEEE Trans. Electron Devices, vol. 55, no. 10, pp. 2614-2622, Oct. 2008, ISSN: 0018-9383.
7. V. D. Maheta, C. Olsen, K. Ahmed and S. Mahapatra, "The Impact of Nitrogen Engineering in Silicon Oxynitride Gate Dielectric on Negative Bias Temperature Instability of p-MOSFETs: A study by Ultra-Fast On-The-Fly IDLIN Technique," IEEE Trans. Electron Devices, vol. 55, no. 7, pp. 1630-1638, Jul. 2008, ISSN:0018-9383.

Conferences and Workshops Publications:

1. H. Liyanage and V. D. Maheta, "License Plate Number Extraction using Mat Lab" in IEEE proc., 9th GCC Int. Conf. and Exhibition , pp. 488-493, 2017.
2. M. AL-Mashaikhi and V. D. Maheta, "Smart Taxi Caller System", Elsevier proc., Int. Conf. on Applied ICT, pp. 455-460, 2014, ISBN: 978-93-5107-285-0.
3. M. Khalik and V. D. Maheta, "Smart Energy Saving System for Lecture Hall", Elsevier proc., Int. Conf. on Applied ICT, pp. 719-725, 2014, ISBN: 978-93-5107-285-0.
4. H. Afzal, and V. D. Maheta, "Low cost smart phone controlled car security system", in IEEE proc., Int. Conf. on Industrial Technology, pp. 670-675, 2014.
5. S. Mahapatra, A. E. Islam, S. Deora, V. D. Maheta, K. Joshi, A. Jain and M. A. Alam, " A critical re-evaluation of the usefulness of R-D framework in predicting NBTI stress and recovery" in IEEE proc., Int. Reliability Physics Symp.,pp.6A.3.1-6A.3.10, 2011, ISSN: 1541-7026, Print ISBN: 978-1-4244-9113-1, E-ISBN: 978-1-4244-9113-7.
6. S. Mahapatra, A. E. Islam, S. Deora, V. D. Maheta, K. Joshi, and M. A. Alam, "Characterization and modeling of NBTI stress, recovery, material dependence and AC degradation using R-D framework" in IEEE proc., Int. Symp. On the Physical & Failure Analysis of Integrated Circuits, pp. 1-7, 2011, ISSN: 1946-1542, Print ISBN: 978-1-4577-0159-7, E-ISBN: 978-1-4577-0159-0.
7. S. Deora, V. D. Maheta, and S. Mahapatra, "NBTI lifetime prediction in SiON p-MOSFETs by H/H2 Reaction-Diffusion(R-D) and dispersive hole trapping model", in IEEE proc., Int. Reliability Physics Symp.,p. 1105-1114, 2010, ISSN: 1541-7026, Print ISBN: 978-1-4244-5430-3.
8. A. E. Islam, S. Mahapatra, S. Deora, V. D. Maheta and M. A. Alam, "On the differences between ultra-fast NBTI measurements and reaction-diffusion theory", in IEEE proc., Int. Electron Device Meeting, p. 733, 2009, Print ISBN: 978-1-4244-5639-0, E-ISBN: 978-1-4244-5640-6.
9. G. Kappila, K. Neeraj, V. D. Maheta and S. Mahapatra, "A Comprehensive Study of Flicker Noise in Plasma Nitrided SiON p-MOSFETs: Process Dependence of Pre-existing and NBTI Stress Generated Trap Distribution Profiles", in IEEE proc., Int. Electron Device Meeting, pp. 103-106, 2008, ISSN: 8164-2284, Print ISBN: 978-1-4244-2377-4, E-ISBN: 978-1-4244-2378-1.

10. S. Mahapatra and V. D. Maheta, "Gate Insulator Process Dependent NBTI in SiON p-MOSFETs,", in IEEE proc., Int. conf. on Solid-state and Integrated-circuit Technology, pp. 616-619, 2008, Print ISBN: 978-1-4244-2185-5, E-ISBN: 978-1-4244-2186-2.
11. V. D. Maheta, C. Olsen, K. Ahmed and S. Mahapatra, "The Impact of Gate Dielectric Nitridation Methodology on NBTI of SiON pMOSFETs: As Study by UF-OTF Technique," in IEEE proc., Int. Symp. On the Physical & Failure Analysis of Integrated Circuits, pp. 1-5, 2008, Print ISBN: 978-1-4244-2039-1, E-ISBN: 978-1-4244-2040-7.
12. A. E. Islam, V. D. Maheta, H. Das, S. Mahapatra, and M. A. Alam, "Mobility degradation due to interface traps in Plasma Oxinitride PMOS devices", in IEEE proc., Int. Reliability Physics Symp., pp. 87-96, 2008, Print ISBN: 978-1-4244-2049-0, E-ISBN: 978-1-4244-2050-6.
13. A. E. Islam, E. N. Kumar, H. Das, S. Purawat, V. Maheta, H. Aono, E. Murakami, S. Mahapatra and M. A. Alam, "Theory and practice of ultra-fast measurements for NBTI degradation: Challenges and opportunities", in IEEE proc., Int. Electron Device Meeting, pp. 805-808, 2007, Print ISBN: 978-1-4244-1507-6, E-ISBN: 978-1-4244-1508-3. (Nominated for Roger A. Haken Best Student Paper Award)
14. E. N. Kumar, V. D. Maheta, S. Purawat, A. E. Islam, C. Olsen, K. Ahmed, M. Alam and S. Mahapatra, "Material dependence of NBTI physical mechanism in silicon oxynitride (SiON) p-MOSFETs: A comprehensive study by ultra-fast On-the-fly (UF-OTF) IDLIN technique", in IEEE proc., Int. Electron Device Meet., pp. 809-812, 2007, Print ISBN: 978-1-4244-1507-6, E-ISBN: 978-1-4244-1508-3.
15. V. D. Maheta, S. Purawat and G. Gupta, "Comparision of Negative Bias Temperature Instability in HfSiO(N)/TaN and SiON/poly-Si pMOSFETs," in IEEE proc., Int. Symp. On the Physical & Failure Analysis of Integrated Circuits, pp. 91-95, 2007, Print ISBN: 978-1-4244-1015-6, E-ISBN: 978-1-4244-1015-6.

Research and Scholarly Contributions:

- **Ph.D. Research**: Negative Bias Temperature Instability (NBTI) for SiON p-MOSFETs
- **M. E. Research**: Validation of Signal Processor for Telephone Signal Handling

Software Tools:

Quartus, QSYS, Eclipse, Modelsim and Xilinx Digital system Design tools, SPICE, Microwind, Multisim, Tinker Cad

Professional Association:

- Indian Society of Technical Education (ISTE) - Life Member

Experience:

- More than 18 years of teaching experience at under graduate level in various engineering institutes in India and abroad.
- Taught modules at post graduate level (M.Sc in Electronics Engineering affiliated with Coventry University, UK) and guided M.Sc Projects.
- Two years of teaching experience as a visiting faculty at post-graduation institute named "Institute of Science & Technology for Advanced Studies & Research (ISTAR)" affiliated to Sardar Patel University at Vallabh Vidyanagar, Gujarat, India.

Responsibilities Handled:

Institute level IQAC team member, Co-chair of 5th, 6th and 7th International Conference on Engineering, Research and Innovations, Institute level program co-ordinator of Remote Center of MNIT Jaipur, Department

level IQAC co-ordinator

Talks/Guest Lectures Delivered:

1. Invited to deliver a talk on “Material Dependence of NBTI in SiON pFETs” to research community at Nanyang Technological University, Singapore.
2. Invited to speak on “Recent trends in VLSI” at A. D. Patel Institute of Technology, Vallabh Vidyanagar.
3. Invited to deliver an expert talk on “Digital Design Using Verilog HDL” at Birla Vishwakarma Mahavidyalaya, Vallabh Vidyanagar.
4. Invited to speak on “Mixed Signal VLSI Design” to post graduate (M. Tech.) students at Nirma Institute of Technology, Ahmedabad.

SESSION CHAIR/JUDGE:

1. Worked as a jury member of paper presentation competition for Brahmastra’09 at Vallabh Vidyanagar.

Declaration
I hereby declare that the foregoing information are correct and complete to the best of my knowledge.

Dr. Vrajesh D. Maheta

Place: Navi Mumbai